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What is claimed is :

1. An electrically conductive layer comprising a copper alloy which includes at least one of Ag, As, Bi, P, Sb, Si, and Ti at not less than 0.1 percent by weight.

2. The electrically conductive layer as claimed in claim 1, wherein said at least one of Ag, As, Bi, P, Sb, Si, and Ti is included in said copper alloy in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper, so that said copper alloy is in a solid solution.

3. The electrically conductive layer as claimed in claim 2, wherein said copper alloy further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

4. The electrically conductive layer as claimed in claim 2, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

5. The electrically conductive layer as claimed in claim 3, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

6. The electrically conductive layer as claimed in claim 2, wherein said copper alloy further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper.

7. The electrically conductive layer as claimed in claim 6, wherein said copper alloy further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

8. The electrically conductive layer as claimed in claim 6, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

9. The electrically conductive layer as claimed in claim 7, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

10. The electrically conductive layer as claimed in claim 2, wherein said electrically conductive layer comprises an interconnection layer within a groove in an insulation layer.

11. The electrically conductive layer as claimed in claim 10, wherein said interconnection layer exists on a barrier metal layer extending on a bottom and side walls of said groove.

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12. An electrically conductive layer comprising a copper alloy which includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

13. The electrically conductive layer as claimed in claim 12, wherein said copper alloy further includes at least one of Ag, As, Bi, P, Sb, Si, and Ti in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper.

14. The electrically conductive layer as claimed in claim 12, wherein said copper alloy further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper.

15. The electrically conductive layer as claimed in claim 13, wherein said copper alloy further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper.

16. The electrically conductive layer as claimed in claim 12, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

17. The electrically conductive layer as claimed in claim 13, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

18. The electrically conductive layer as claimed in claim 14, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

19. The electrically conductive layer as claimed in claim 15, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

20. The interconnection layer as claimed in claim 12, wherein said electrically conductive layer comprises an interconnection layer within a groove in an insulation layer.

21. The interconnection layer as claimed in claim 20, wherein said interconnection layer exists on a barrier metal layer extending on a bottom and side walls of said groove.

22. A semiconductor device comprising :

a semiconductor substrate ;

an insulation layer over said semiconductor substrate, and said insulation layer having a groove ;

a barrier metal layer on a bottom and side walls of said groove ; and

an interconnection layer on said barrier metal layer, and said interconnection layer filling said groove,

wherein said interconnection layer comprises a copper alloy which includes at least one of Ag, As, Bi, P, Sb, Si, and Ti in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper, so that said copper alloy is in a solid solution.

23. The semiconductor device as claimed in claim 22, wherein said copper alloy further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

24. The semiconductor device as claimed in claim 22, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

25. The semiconductor device as claimed in claim 23, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

26. The semiconductor device as claimed in claim 22, wherein said copper alloy further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to not more than a maximum solubility

limit to copper.

27. The semiconductor device as claimed in claim 26, wherein said copper alloy further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

28. The semiconductor device as claimed in claim 26, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

29. The semiconductor device as claimed in claim 27, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

30. A semiconductor device comprising :

a semiconductor substrate ;

an insulation layer over said semiconductor substrate, and said insulation layer having a groove ;

a barrier metal layer on a bottom and side walls of said groove ; and

an interconnection layer on said barrier metal layer, and said interconnection layer filling said groove,

wherein said interconnection layer comprises a copper alloy which includes at least one of Mo, Ta and W in a range of not less than 0.1

percent by weight to not more than 1 percent by weight.

31. The semiconductor device as claimed in claim 30, wherein said copper alloy further includes at least one of Ag, As, Bi, P, Sb, Si, and Ti in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper.

32. The semiconductor device as claimed in claim 30, wherein said copper alloy further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper.

33. The semiconductor device as claimed in claim 31, wherein said copper alloy further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper.

34. The semiconductor device as claimed in claim 30, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

35. The semiconductor device as claimed in claim 31, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

36. The semiconductor device as claimed in claim 33, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

37. The semiconductor device as claimed in claim 34, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

38. A method of forming a semiconductor device, comprising the steps of :

forming a groove in an insulation layer over a semiconductor substrate ;

forming a barrier metal layer on a bottom and side walls of said groove ;

forming a seed copper layer including at least one of Ag, As, Bi, P, Sb, Si, and Ti on said barrier metal layer ;

forming a copper layer on said seed copper layer so that laminations of said barrier metal layer, said seed copper layer and said copper layer fill within said groove ; and

carrying out a heat treatment to form an interconnection layer on said barrier metal layer,

wherein said interconnection layer comprises a copper alloy which includes at least one of Ag, As, Bi, P, Sb, Si, and Ti in a range of not

less than 0.1 percent by weight to not more than a maximum solubility limit to copper, so that said copper alloy is in a solid solution.

39. The method as claimed in claim 38, further comprising the step of selectively removing said copper layer, so that said copper layer remains only within said groove before said heat treatment is carried out.

40. The method as claimed in claim 38, further comprising the step of selectively removing said interconnection layer, so that said interconnection layer remains only within said groove after said heat treatment has been carried out.

41. The method as claimed in claim 38, wherein said seed copper layer further includes at least one of Mo, Ta and W, so that said interconnection layer further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

42. The method as claimed in claim 38, wherein said seed copper layer further includes at least one of Cr and Ni, so that said interconnection layer further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

43. The method as claimed in claim 41, wherein said seed copper

layer further includes at least one of Cr and Ni, so that said interconnection layer further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

44. The method as claimed in claim 38, wherein said seed copper layer further includes at least one of Ge and Mg, so that said interconnection layer further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper.

45. The method as claimed in claim 44, wherein said seed copper layer further includes at least one of Mo, Ta and W, so that said interconnection layer further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

46. The method as claimed in claim 44, wherein said seed copper layer further includes at least one of Cr and Ni, so that said interconnection layer further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

47. The method as claimed in claim 45, wherein said seed copper layer further includes at least one of Cr and Ni, so that said interconnection layer further includes at least one of Cr and Ni in a range of not less than

0.1 percent by weight to not more than 1 percent by weight.

48. A method of forming a semiconductor device, comprising the steps of :

forming a groove in an insulation layer over a semiconductor substrate ;

forming a barrier metal layer on a bottom and side walls of said groove ;

forming a seed copper layer including at least one of Mo, Ta and W on said barrier metal layer ;

forming a copper layer on said seed copper layer so that laminations of said barrier metal layer, said seed copper layer and said copper layer fill within said groove ; and

carrying out a heat treatment to form an interconnection layer on said barrier metal layer,

wherein said interconnection layer comprises a copper alloy which includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

49. The method as claimed in claim 48, further comprising the step of selectively removing said copper layer, so that said copper layer remains only within said groove before said heat treatment is carried out.

50. The method as claimed in claim 48, further comprising the step

of selectively removing said interconnection layer, so that said interconnection layer remains only within said groove after said heat treatment has been carried out.

51. The method as claimed in claim 48, wherein said seed copper layer further includes at least one of Ag, As, Bi, P, Sb, Si, and Ti, so that said interconnection layer further includes at least one of Ag, As, Bi, P, Sb, Si, and Ti in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper.

52. The method as claimed in claim 48, wherein said seed copper layer further includes at least one of Ge and Mg, so that said interconnection layer further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper.

53. The method as claimed in claim 51, wherein said seed copper layer further includes at least one of Ge and Mg, so that said interconnection layer further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper.

54. The method as claimed in claim 48, wherein said seed copper layer further includes at least one of Cr and Ni, so that said interconnection

layer further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

55. The method as claimed in claim 51, wherein said seed copper layer further includes at least one of Cr and Ni, so that said interconnection layer further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

56. The method as claimed in claim 53, wherein said seed copper layer further includes at least one of Cr and Ni, so that said interconnection layer further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

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